LISTING OF THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in this application.

1. (Currently Amended) A method of controlling a processor comprising:

consulting a table that lists a plurality of operation points defined by combinations, wherein each comprises ~~each comprising~~:

a) the number of a plurality of subprocessors ~~processing blocks~~ formed inside a processor [[and]] that are in operation; and

b) one of a plurality of operating frequencies available for use by switching, so as to switch between the operation points in accordance with a temperature.

2. (Cancelled)

3. (Currently Amended) The method of controlling a processor according to claim 1, comprising allocating tasks in consideration of the number of the subprocessors ~~processing blocks~~ available in parallel, the number being determined task by task.

4. (Currently Amended) The method of controlling a processor according to claim 1, comprising allocating tasks to at least a subprocessor ~~processing block~~ having a lowest temperature among the subprocessors ~~processing blocks~~.

5. (Currently Amended) The method of controlling a processor comprising: consulting a table that lists a plurality of operation points defined by combinations, wherein each comprises ~~each comprising~~:

a) the number of subprocessors ~~processing blocks~~ formed inside a processor [[and]] that are in operation; and

b) one of a plurality of operating frequencies available for use by switching, so as to switch between the operation points.

6. (Previously Presented) A method of controlling a processor according to claim 5, wherein the table lists the plurality of operation points in order of processing performance.

7. (Previously Presented) The method of controlling a processor according to claim 6, wherein when the processor is predicted to exceed or exceeds a predetermined threshold in temperature, an operation point yielding a smaller amount of heat generation than that of an operation point selected currently is detected out of the operation points, so that the operation point selected currently is switched to the operation point detected.

8. (Previously Presented) The method of controlling a processor according to claim 7, wherein when a plurality of operation points are detected, the operation point selected currently is switched to a operation point yielding maximum performance.

9. (Currently Amended) A processor comprising:

a plurality of subprocessors ~~processing blocks~~;

a sensor, which measures a temperature;

a table that lists a plurality of operation points defined by combinations, wherein each comprises ~~each comprising~~: a) the number of subprocessors ~~processing blocks~~ in operation; and b) one of a plurality of operating frequencies available for use by switching; and

a control unit, which consults the table and switches between the operation points in accordance with the measured temperature.

10. (Cancelled)

11. (Currently Amended) The processor according to claim 9, wherein the control unit allocates tasks in consideration of the number of the plurality of subprocessors ~~processing blocks~~ available in parallel, the number being determined task by task.

12. (Currently Amended) The processor according to claim 9, wherein the control unit allocates tasks to at least a subprocessor ~~processing block~~ having a lowest temperature among the plurality of subprocessors ~~processing blocks~~.

13. (Currently Amended) A processor comprising:

a plurality of subprocessors ~~processing blocks~~;

a table, which lists a plurality of operation points defined by combinations, wherein each comprises ~~each comprising~~: a) the number of subprocessors ~~processing blocks~~ in operation; and b) one of a plurality of operating frequencies available for use by switching; and

a control unit, which consults the table and switches between the operation points as appropriate.

14. (Previously Presented) The processor according to claim 13, wherein the table lists processing performance for each of the combinations.

15. (Previously Presented) The processor according to claim 14, wherein when the processor is predicted to exceed or exceeds a predetermined threshold in temperature, the control unit selects an operation point yielding a smaller amount of heat generation than at present out of the operation points, and switches to the operation point selected.

16. (Currently Amended) An information processing apparatus comprising a processor, which executes various tasks,

the processor including:

a plurality of subprocessors ~~processing blocks~~;

a sensor, which measures a temperature;

a table that lists a plurality of operation points defined by combinations, where each comprises ~~each comprising~~: a) the number of subprocessors ~~processing blocks~~ in operation; and b) one of a plurality of operating frequencies available for use by switching; and

a control unit, which consults the table and switches between the operation points in accordance with the measured temperature.

17. (Cancelled)

18. (Currently Amended) The information processing apparatus according to claim 16, wherein the control unit allocates tasks in consideration of the number of the plurality of subprocessors ~~processing blocks~~ available in parallel, the number being determined task by task.

19. (Currently Amended) The information processing apparatus according to claim 16, wherein the control unit allocates tasks to at least a subprocessor ~~processing block~~ having a lowest temperature among the plurality of subprocessors ~~processing blocks~~.

20. (Currently Amended) An information processing apparatus comprising a processor, which executes various tasks,

the processor including:

a plurality of subprocessors ~~processing blocks~~;

a table, which lists a plurality of operation points defined by combinations, where each comprises ~~each comprising~~: a) the number of subprocessors ~~processing blocks~~ in operation; and b) one of a plurality of operating frequencies available for use by switching; and

a control unit, which consults the table and switches between the operation points as appropriate.

21. (Currently Amended) An information processing system comprising a processor, which executes various tasks,

the processor including:

a plurality of subprocessors ~~processing blocks~~;

a sensor, which measures a temperature;

a table, which lists a plurality of operation points defined by combinations, wherein each comprises ~~each comprising~~: a) the number of subprocessors ~~processing blocks~~ in operation; and b) one of a plurality of operating frequencies available for use by switching; and

a control unit, which consults the table and switches between the operation points in accordance with the measured temperature.

22. (Cancelled)

23. (Currently Amended) The information processing system according to claim 21, wherein the control unit allocates tasks in consideration of the number of the plurality of subprocessors ~~processing blocks~~ available in parallel, the number being determined task by task.

24. (Currently Amended) The information processing system according to claim 21, wherein the control unit allocates tasks to at least a subprocessor ~~processing block~~ having a lowest temperature among the plurality of subprocessors ~~processing blocks~~.

25. (Currently Amended) An information processing system comprising a processor, which executes various tasks,

the processor including:

a plurality of subprocessors ~~processing blocks~~;

a table, which lists a plurality of operation points defined by combinations, wherein each comprises ~~each comprising~~: a) the number of subprocessors ~~processing blocks~~ in operation; and b) one of a plurality of operating frequencies available for use by switching; and

a control unit, which consults the table and switches between the operation points as appropriate.

26. (Currently Amended) A processor readable storage medium having stored thereon a processor control program comprising instructions for:

consulting a table that lists a plurality of operation points defined by combinations, wherein each comprises ~~each comprising~~: a) the number of subprocessors ~~processing blocks~~ formed inside a processor in operation; and b) one of a plurality of operating frequencies available for use by switching, and

switching between the operation points in accordance with a temperature.

27. (Cancelled)

28. (Currently Amended) The processor readable storage medium according to claim 26, further comprising instructions for allocating tasks in consideration of the number of the plurality of subprocessors ~~processing blocks~~ available in parallel, the number being determined task by task.

29. (Currently Amended) The processor readable storage medium according to claim 26, further comprising instructions for allocating tasks to at least a subprocessor ~~processing block~~ having a lowest temperature among the plurality of subprocessors ~~processing blocks~~.

30. (Currently Amended) A processor readable storage medium comprising a processor control program comprising instructions for:

consulting a table that lists a plurality of operation points defined by combinations, wherein each comprises ~~each comprising~~: a) the number of subprocessors ~~processing blocks~~ formed inside a processor in operation; and b) one of a plurality of operating frequencies available for use by switching, and

switching between the operation points.

31. (Currently Amended) The method of controlling a processor according to claim 3, comprising allocating tasks to at least a subprocessor ~~processing block~~ having a lowest temperature among the plurality of subprocessors ~~processing blocks~~.

32. (Currently Amended) The processor according to claim 11, wherein the control unit allocates tasks to at least a subprocessor ~~processing block~~ having a lowest temperature among the plurality of subprocessors ~~processing blocks~~.

33. (Currently Amended) The information processing apparatus according to claim 18, wherein the control unit allocates tasks to at least a subprocessor ~~processing block~~ having a lowest temperature among the plurality of subprocessors ~~processing blocks~~.

34. (Currently Amended) The information processing system according to claim 23, wherein the control unit allocates tasks to at least a subprocessor ~~processing block~~ having a lowest temperature among the plurality of processing tasks.

35. (Currently Amended) The processor readable storage medium according to claim 28, further comprising instructions for allocating tasks to at least a subprocessor ~~processing block~~ having a lowest temperature among the plurality of processing tasks.